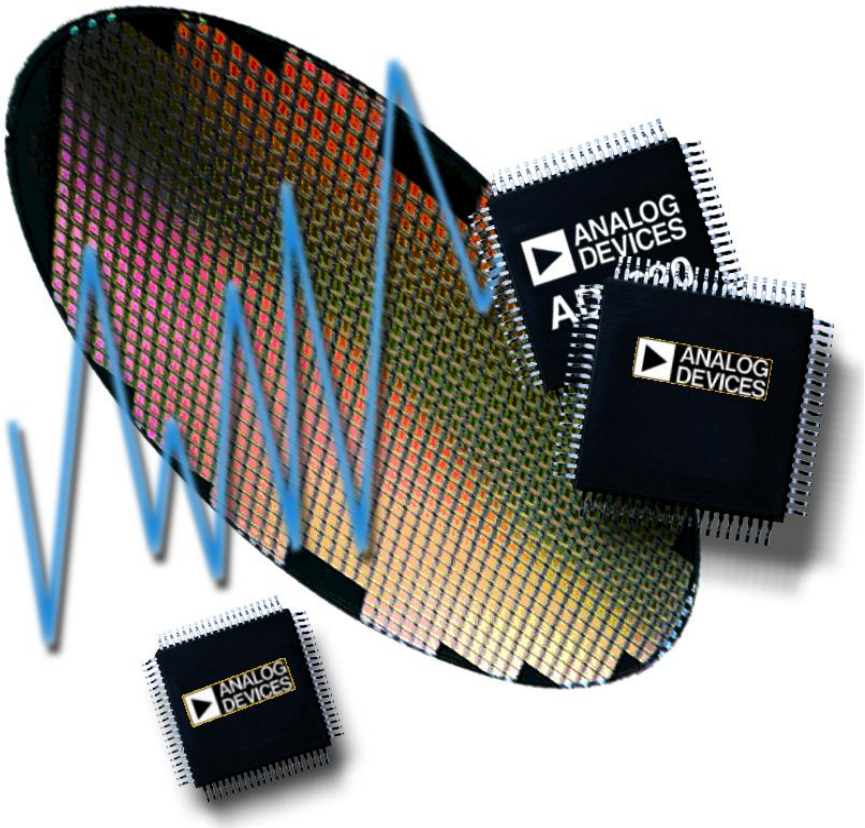

Reliability Report

Report Title: ADuM4190 Enhanced Product Gold Coil Pad Size Reduction Qualification

Report Number: 18435

Revision: A

Date: 6 September 2022

Summary

This report documents the successful completion of the reliability qualification requirements for the release of the ADuM4190 product change in a 16-SOIC_IC package. The ADuM4190 is an isolated error amplifier based on iCoupler® technology.

Unlike optocoupler-based solutions, which have an uncertain current transfer ratio over lifetime and at high temperature, the ADuM4190 transfer function does not change over its lifetime, and it is stable over a wide temperature range of -40^{0}C to +125^{0}C

The change being qualified is the decrease of dimensions of two bond pads on the Transformer Coil die.

The ADuM4190 is a 2-die architecture product:

- Die 1 (TMEC54) is fabed on 0.35um DMOS at TSMC and post-processed at ADI-Limerick with 1M (2x10um) Polyimide Isolation.
- Die 2 (TMEC53) is fabed on 0.35um DMOS at TSMC

Table 1: ADuM4190EP Product Characteristics

Die/Fab

Die Id	TMEC54A / 8EM15E01	TMEC53A-T1
Die Name	ADuM3190TC	ADuM3190IC
Die Size (mm)	0.90 x 2.40	0.90 x 2.40
Wafer Fabrication Site	TSMC Fab-3C / ADI-Limerick	TSMC Fab-3C
Wafer Fabrication Process	0.35µm DMOS / 1M (2x10um) Polyimide Isolation	0.35µm DMOS
Approximate Transistor Count	5,530	6,950
Passivation Layer	undoped-oxide/OxyNitride	undoped-oxide/OxyNitride
Bond Pad Metal Composition	AlCu / Au	AlCu
Polyimide	No	Yes

Package/Assembly

Package	16-SOIC_IC
Body Size (mm)	12.80 x 7.50 x 2.50
Operating Temperature Range	-40°C ≤ TA ≤ 125°C
Assembly Location	ASE Taiwan
Molding Compound	Sumitomo G700LY
Wire Type	Heraeus AW7 4N Gold
Wire Diameter (mils)	1.30
Die Attach	Hitachi EN-4900GC
Lead Frame Material	Copper
Lead Finish	NiPdAu
Moisture Sensitivity Level	3
Maximum Peak Reflow Temperature (°C)	260

Description / Results of Tests Performed

Tables 2 and 3 provide a description of the qualification tests conducted and the associated test results for products manufactured on the same technologies as described in Table 1. All devices were electrically tested before and after each stress. Any device that did not meet all electrical data sheet limits following stressing would be considered a valid (stress-attributable) failure unless there was conclusive evidence to indicate otherwise.

Table 2: SOIC_IC at ASE Taiwan Package Qualification Test Results

Test Name	Specification	Conditions	Device	Lot #	Sample Size	Qty. Failures
High Temperature Storage Life (HTSL) [1]	JESD22-A103	150°C, 1,000 Hours	AD7403	Q11552.HS1	77	0
			ADN4711	Q12587.HS1	45	0
High Temperature Storage Life (HTSL) [2]	JESD22-A103	150°C, 1,000 Hours	ADuM226N0W	Q12583.2	77	0
Highly Accelerated Temperature and Humidity Stress Test (HAST) [3,1]	JESD22-A110	130C 85%RH 33.3 psia, Biased, 96 Hours	AD7403	Q11552.HA1	77	0
				Q11552.HA2	77	0
				Q11552.HA3	77	0
			ADN4711	Q12587.HA1	77	0
				Q12587.HA2	77	0
				Q12587.HA3	77	0
Highly Accelerated Temperature and Humidity Stress Test (HAST) [3,2]	JESD22-A110	130C 85%RH 33.3 psia, Biased, 96 Hours	ADuM226N0W	Q12583.1	77	0
				Q12583.11	77	0
				Q12583.4	77	0
Low Temperature Storage (LTS) [1]	JESD22-A119	-55°C, 1,000 Hours	AD7403	Q11552.LS1	77	0
				Q11552.LS2	77	0
				Q11552.LS3	77	0
Solder Heat Resistance (SHR) [3,4]	J-STD-020	MSL-3	ADuM4190	Q14891.1	11	0
				Q14891.3	11	0
				Q14891.5	11	0
Temperature Cycling (TC) [3,1]	JESD22-A104	-65°C/+150°C, 1,000 Cycles	AD7403	Q11552.TC1	77	0
				Q11552.TC2	77	0
				Q11552.TC3	77	0
Temperature Cycling (TC) [3,9]	JESD22-A104	-65°C/+150°C, 1,000 Cycles	ADuM4190	Q18435.1.1	77	0
				Q18435.2.1	77	0
				Q18435.3.1	77	0
Temperature Cycling (TC) [3,2]	JESD22-A104	-65°C/+150°C, 1,000 Cycles	ADuM4190EP	Q11906.2	77	0
				Q11906.3	77	0
Unbiased HAST (UHST) [3,1]	JESD22-A118	130C 85%RH 33.3 psia, 96 Hours	AD7403	Q11552.UH1	77	0
				Q11552.UH2	77	0
				Q11552.UH3	77	0
Unbiased HAST (UHST) [3,6]	JESD22-A118	130C 85%RH 33.3 psia, 96 Hours	ADuM4120	Q12379.10	77	0
				Q12379.11	77	0
				Q12379.9	77	0
			ADuM4121	Q11822.12	77	0
				Q11822.13	77	0
				Q11822.14	77	0

[1] Electrical test was performed at Room/HV

[2] Pre- and post-stress electrical test was performed at room and hot temperatures.

[3] These samples were subjected to preconditioning (per J-STD-020 Level 3) prior to the start of the stress test. Level 3 preconditioning consists of the following: Bake: 24 hrs @ 125°C, Unbiased Soak: 192 hrs @ 30°C, 60%RH, Reflow: 3 passes through an oven with a peak temperature of 260°C.

[4] Electrical test was performed at Room.

[5] These samples were subjected to preconditioning (per J-STD-020 Level 1) prior to the start of the stress test. Level 1 preconditioning consists of the following: Bake: 24 hrs @ 125°C, Unbiased Soak: 168 hrs @ 85°C, 85%RH, Reflow: 3 passes through an oven with a peak temperature of 260°C.

[6] Electrical test was performed at room temperature.

[7] Electrical test was performed at Hot.

[8] Post-TCT wire bond pull testing was performed per AEC-Q100 on five devices from TCT lot Q14891.6. Complete data for the five units are presented in Appendix A of this report.

[9] Pre- and post-stress electrical test was performed at hot, room and cold temperatures.

Table 3: 0.35µm DMOS at TSMC Fab-3C Fab Qualification Test Results

Test Name	Specification	Conditions	Device	Lot #	Sample Size	Qty. Failures
Early Life Failure Rate (ELFR) [1]	MIL-STD-883, M1015	125°C, 48 Hours	ADuM3190	Q12803.10	77	0
				Q12803.11	77	0
				Q12803.12	41	0
				Q12803.13	77	0
				Q12803.14	77	0
				Q12803.15	77	0
				Q12803.16	77	0
				Q12803.17	77	0
				Q12803.18	77	0
				Q12803.19	77	0
				Q12803.20	77	0
				Q12803.21	77	0
				Q12803.22	77	0
				Q12803.24	77	0
				Q12803.25	77	0
				Q12803.26	77	0
				Q12803.27	77	0
				Q12803.28	77	0
				Q12803.29	77	0
				Q12803.3	77	0
				Q12803.30	77	0
				Q12803.31	77	0
				Q12803.32	77	0
				Q12803.33	77	0
				Q12803.34	6	0
				Q12803.35	16	0
				Q12803.36	6	0
				Q12803.4	77	0
				Q12803.5	77	0
				Q12803.6	77	0
				Q12803.7	77	0
				Q12803.8	77	0
				Q12803.9	77	0
High Temperature Operating Life (HTOL) [1, 5]	JESD22-A108	125°C<Tj<135°C, Biased, 1,000 Hours	ADuM4190	Q11215.1	77	0
		150°C<Tj<175°C, Biased, 500 Hours	ADuM3190	Q12803.1	77	0
				Q12803.2	77	0
				Q12803.23	77	0
High Temperature Operating Life (HTOL) [1, 4]	JESD22-A108	150°C<Tj<175°C, Biased, 500 Hours	ADuM3472	Q8395.13	77	0
				Q8395.7	77	0
High Temperature Operating Life (HTOL) [2, 5]	JESD22-A108	125°C<Tj<135°C, Biased, 1,000 Hours	ADuM3190W	Q11592.18	77	0
				Q11592.5	77	0
				Q11592.9	77	0
High Temperature Storage Life (HTSL) [3]	JESD22-A103	150°C, 1,000 Hours	ADuM3190W	Q11592.8	77	0
Highly Accelerated Temperature and Humidity Stress Test	JESD22-A110	130C 85%RH 33.3 psia, Biased, 96 Hours	ADuM3472	Q8395.10	77	0

Test Name	Specification	Conditions	Device	Lot #	Sample Size	Qty. Failures
(HAST) [4,1]						
Highly Accelerated Temperature and Humidity Stress Test (HAST) [5,1]	JESD22-A110	130C 85%RH 33.3 psia, Biased, 96 Hours	ADuM4474	Q9720.HA1	77	0
Highly Accelerated Temperature and Humidity Stress Test (HAST) [5,6]	JESD22-A110	130C 85%RH 33.3 psia, Biased, 96 Hours	ADuM3190	Q12752.HA1	77	0
				Q12752.HA2	77	0
				Q12752.HA3	77	0
				Q12752.HA4	77	0
Highly Accelerated Temperature and Humidity Stress Test (HAST) [5,3]	JESD22-A110	130C 85%RH 33.3 psia, Biased, 96 Hours	ADuM3190W	Q11592.6	77	0
				Q11592.7	77	0
				Q13202.23	77	0

[1] Electrical test was performed at room temperature.

[2] Pre- and post-stress electrical test was performed at hot, room and cold temperatures.

[3] Pre- and post-stress electrical test was performed at room and hot temperatures.

[4] These samples were subjected to preconditioning (per J-STD-020 Level 1) prior to the start of the stress test. Level 1 preconditioning consists of the following: Bake: 24 hrs @ 125°C, Unbiased Soak: 168 hrs @ 85°C, 85%RH, Reflow: 3 passes through an oven with a peak temperature of 260°C.

[5] These samples were subjected to preconditioning (per J-STD-020 Level 3) prior to the start of the stress test. Level 3 preconditioning consists of the following: Bake: 24 hrs @ 125°C, Unbiased Soak: 192 hrs @ 30°C, 60%RH, Reflow: 3 passes through an oven with a peak temperature of 260°C.

[6] Electrical test was performed at Room/Hot/HV First&Last.

Samples of the many devices manufactured with these package and process technologies are continuously undergoing reliability evaluation as part of the ADI Reliability Monitor Program. Additional qualification data is available on Analog Devices' web site.

ESD Test Results

The results of Human Body Model (HBM) and Field-Induced Charged Device Model (FICDM) ESD testing are summarized in Table 4. ADI measures ESD results using stringent test procedures based on the specifications listed. Any comparison with another supplier's results should ensure that the same ESD test procedures have been used. For further details, please see the EOS/ESD chapter of the ADI Reliability Handbook (available via the 'Quality and Reliability' link on Analog Devices' web site).

Table 4: ADuM4190 ESD Test Results

ESD Model	Package	ESD Test Spec	RC Network	Highest Pass Level	First Fail Level	Class
FICDM	16-SOIC_IC	JS-002	1Ω, Cpkg	±1250V	NA	C3
HBM	16-QSOP	ESDA/JEDEC JS-001-2011	1.5kΩ, 100pF	±4000V	NA	3A

Latch-Up Test Results

Three samples of the ADuM4190EP were latch-up tested at T_A=125°C per JEDEC Standard JESD78, Class II. Pre- and post-stress electrical test was performed at room and hot temperatures. All pins passed.

Passing Positive Current	Passing Negative Current	Passing Over-Voltage
+100mA	-100mA	+24V

Approvals

Reliability Engineer: Alex Shepetovskiy

Additional Information

Data sheets and other additional information are available on Analog Devices' web site

Appendix

Post TCT Wire Bond Pull Test Results

Appendix A

Post-TCT Wire Bond Pull Test Results

Post TCT - Q14891.9 - ADuM4190										
Device	**1**		**2**		**3**		**4**		**5**	
Wire	**PULL (gf)**	**Mode**	**PULL (gf)**	**Mode**	**PULL (gf)**	**Mode**	**PULL (gf)**	**Mode**	**PULL (gf)**	**Mode**
1	13.231	1	13.17	1	13.21	1	13.349	1	14.022	1
2	16.141	1	15.244	1	16.207	1	16.265	1	16.23	1
3	15.006	1	15.23	1	15.945	1	16.582	1	16.264	1
4	14.152	1	14.128	1	14.362	1	14.572	1	13.594	1
5	14.993	1	15.017	1	15.634	1	15.222	1	14.946	1
6	14.958	1	14.519	1	15.075	1	14.843	1	15.354	1
7	13.665	1	13.885	1	14.47	1	13.791	1	14.243	1
8	14.213	1	13.098	1	13.368	1	13.383	1	13.607	1
9	9.4626	2	9.5505	2	11.849	2	9.8867	2	9.644	4
10	9.4749	2	7.9083	4	6.0556	4	9.7153	2	9.0881	4
11	12.684	1	13.44	1	13.035	1	14.304	1	13.301	1
12	14.134	1	13.91	1	13.91	1	14.17	1	13.679	1
13	14.894	1	14.104	1	15.189	1	13.713	1	15.258	1
14	14.429	1	13.874	1	15.232	1	14.153	1	14.604	1
15	14.325	1	13.07	1	14.029	1	13.863	1	13.588	1
16	15.693	1	15.167	1	15.516	1	14.794	1	15.135	1
17	15.742	1	16.337	1	15.65	1	15.532	1	16.462	1
18	13.801	1	14.003	1	13.634	1	13.077	1	13.423	1
Min	**9.46**		**7.91**		**6.06**		**9.72**		**9.09**	
Max	**16.14**		**16.34**		**16.21**		**16.58**		**16.46**	
Ave	**13.94**		**13.65**		**14.02**		**13.96**		**14.02**	
STDEV	**1.80**		**1.95**		**2.24**		**1.74**		**1.92**	

Failure Codes	
0	**Non Destruct**
1	**Neck Break**
2	**Span Break**
3	**Die Interface Break**
4	**Sub Interface Break**
5	**Die Metal Lift**
6	**Sub Metal Lift**
7	**Die Fracture**
8	**Sub Fracture**
9	**No Code assign**
10	**Voided test**
11	**Void User Cancel**
12	**Void Over Travel**
13	**No Code assigned**